**ECE 3663 Design Review 2**

04/09/2012

**Group: ADD**

Chuhong Duan

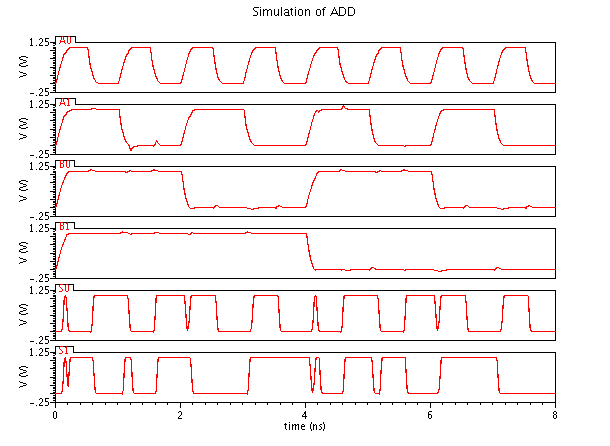
Ian Dansey

Michael Kremer

Lingtian Wan

1. **Simulation results**
2. ADD

We used 2 bits for each input A and B to demonstrate the functionality of the 16-bit adder. Inputs: A1A0, B1B0. Outputs: S1S0.



A1A0=11, B1B0=11: S1S0=10; A1A0=10, B1B0=11: S1S0=01;

A1A0=01, B1B0=11: S1S0=00; A1A0=00, B1B0=11: S1S0=11;

A1A0=11, B1B0=10: S1S0=01; A1A0=10, B1B0=10: S1S0=00;

A1A0=01, B1B0=10: S1S0=11; A1A0=00, B1B0=10: S1S0=10;

A1A0=11, B1B0=01: S1S0=00; A1A0=10, B1B0=01: S1S0=11;

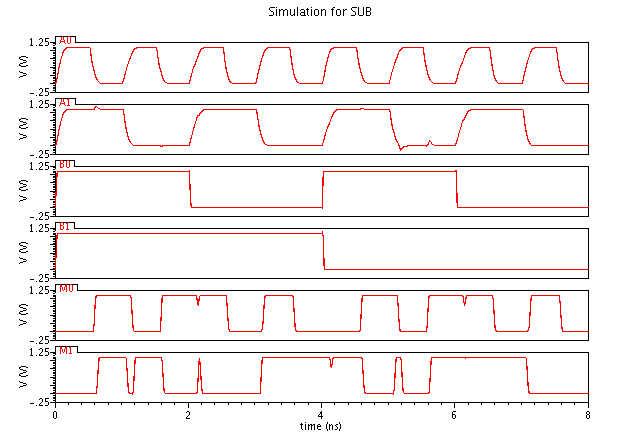
A1A0=01, B1B0=01: S1S0=10; A1A0=00, B1B0=01: S1S0=01;

A1A0=11, B1B0=00: S1S0=11; A1A0=10, B1B0=00: S1S0=10;

A1A0=01, B1B0=00: S1S0=01; A1A0=00, B1B0=00: S1S0=00.

1. SUB

We used 2 bits for each input A and B to demonstrate the functionality of the 16-bit substractor. Inputs: A1A0, B1B0. Outputs: S1S0 = A1A0 – B1B0.



A1A0=11, B1B0=11: S1S0=00; A1A0=10, B1B0=11: S1S0=11;

A1A0=01, B1B0=11: S1S0=10; A1A0=00, B1B0=11: S1S0=01;

A1A0=11, B1B0=10: S1S0=01; A1A0=10, B1B0=10: S1S0=00;

A1A0=01, B1B0=10: S1S0=11; A1A0=00, B1B0=10: S1S0=10;

A1A0=11, B1B0=01: S1S0=10; A1A0=10, B1B0=01: S1S0=01;

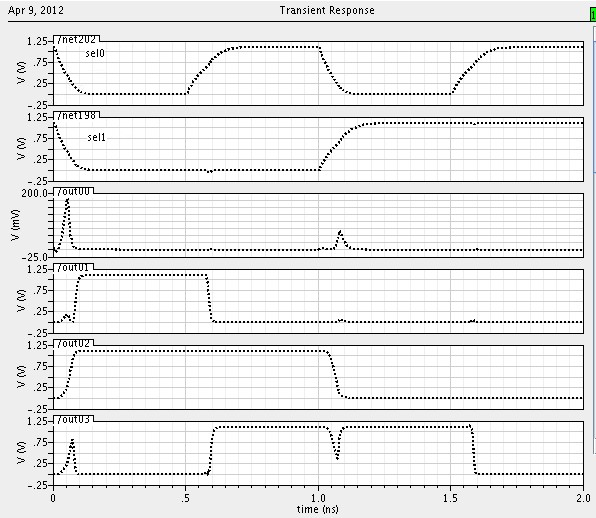
A1A0=01, B1B0=01: S1S0=00; A1A0=00, B1B0=01: S1S0=11;

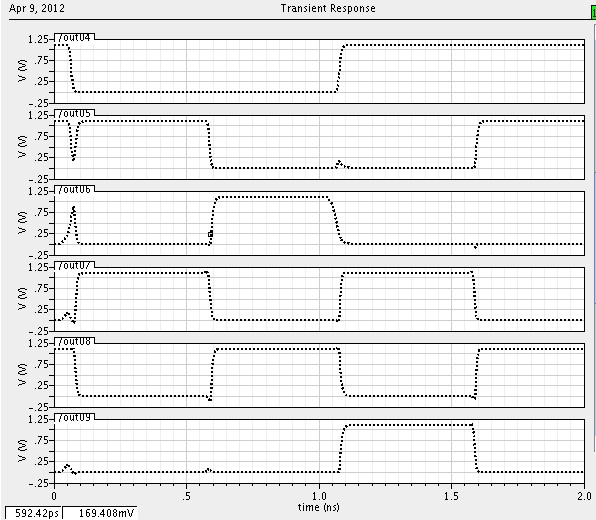
A1A0=11, B1B0=00: S1S0=11; A1A0=10, B1B0=00: S1S0=10;

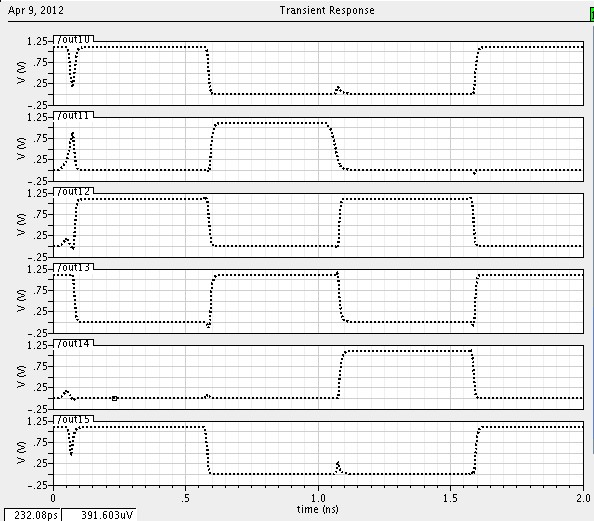
A1A0=01, B1B0=00: S1S0=01; A1A0=00, B1B0=00: S1S0=00.

1. SHIFT

Use input A=1100 1010 0101 0011, input B as pulse signals: sel1 sel0 =00 – 01 – 10 – 11.







Sel1 sel0 = 00: A shifts left by 1bit, output = 100 1010 0101 0011 0;

Sel1 sel0 = 01: A shifts left by 2bits, output = 00 1010 0101 0011 00;

Sel1 sel0 = 10: A shifts left by 3bits, output = 0 1010 0101 0011 000;

Sel1 sel0 = 11: A shifts left by 4bits, output = 1010 0101 0011 0000.

1. Register

We choose inputs D0 and D8 to demonstrate the functionality of the 16-bit rising edge-triggered register.

Outputs are Q0 and Q8. The clock period is 100 psec.

